Docket No. 303.744US1 Micron Ref. No. 00-1198
WD # 474678

CLEAN VERSION OF PENDING CLAIMS

METHOD TO FABRICATE SURFACE P-CHANNEL CMOS
Applicant: Suraj J. Mathew et al.
Serial No.: 09/808,261

Claims 1-50, as of December 19, 2002 (Date of Response to First Office Action).

1. (Amended) A method of forming a transistor, comprising:

forming a gate dielectric layer on a semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the gate dielectric layer;

selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor material on the modified gate dielectric layer and forming a second conductivity type gate from the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gate.

2. The method of claim 1, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the gate dielectric layer.

3. The method of claim 1, wherein the first conductivity type semiconductor layer is formed in-situ.

4. The method of claim 1, wherein the second conductivity type semiconductor layer is formed in-situ.

5. The method of claim 1, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; and depositing a second conductivity type semiconductor material on the gate dielectric.

6. (Amended) A method of forming a transistor, comprising:

forming a first gate dielectric layer on a semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the first gate dielectric layer;

selectively removing a portion of the first conductivity type semiconductor layer to expose the first gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well, the second gate dielectric layer being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor material on the second gate dielectric layer and forming a second conductivity type gate from the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gate.

7. The method of claim 6, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the first gate dielectric layer, before removing the first gate dielectric layer.

8. The method of claim 6, further comprising coupling a hardened dielectric layer to the second gate dielectric layer.

9. The method of claim 6, wherein the second gate dielectric layer differs in thickness from the first gate dielectric layer.

10. The method of claim 6, wherein the first conductivity type semiconductor layer is formed in-situ.

11. The method of claim 6, wherein the second conductivity type semiconductor layer is formed in-situ.

12. The method of claim 6, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; removing the first gate dielectric layer; and depositing a second conductivity type semiconductor material on the second gate dielectric layer.

13. (Amended) A method of forming pair of transistors, comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric layer, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor layer on the modified gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.

14. The method of claim 13, wherein forming a second conductivity type semiconductor well comprises implanting a second conductivity type well through the gate dielectric layer.

15. The method of claim 13, wherein the first conductivity type semiconductor layer is formed in-situ.

16. The method of claim 13, wherein the second conductivity type semiconductor layer is formed in-situ.

17. The method of claim 13, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; and depositing a second conductivity type semiconductor layer.

18. (Amended) A method of forming a pair of transistors, comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a first gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the first gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to

expose the first gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well, the second gate dielectric layer being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor layer on the second gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.

19. The method of claim 18, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the first gate dielectric layer, before removing the first gate dielectric layer.

20. The method of claim 18, further comprising coupling a hardened dielectric layer to the second gate dielectric.

21. The method of claim 18, wherein the second gate dielectric differs in thickness from the first gate dielectric.

22. The method of claim 18, wherein the first conductivity type semiconductor layer is formed in-situ.

23. The method of claim 18, wherein the second conductivity type semiconductor layer is formed in-situ.

24. The method of claim 18, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; removing the first gate dielectric layer; and depositing a second conductivity type semiconductor material on the second gate dielectric layer.

25. A method of forming a semiconductor memory device, comprising:

forming at least one memory array;

forming a number of wordlines coupled to the memory array;

forming a number of bitlines coupled to the memory array;

forming at least one transistor coupled to the memory array comprising:

forming a gate dielectric layer on a semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the gate dielectric layer;

selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

depositing a second conductivity type semiconductor material on the gate dielectric layer and forming a first conductivity type gate from the first conductivity type semiconductor layer; and

forming source/drain regions adjacent the gate.

26. The method of claim 25, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the gate dielectric layer.

27. The method of claim 25, wherein the first conductivity type semiconductor layer is formed in-situ.

28. The method of claim 25, wherein the second conductivity type semiconductor layer is formed in-situ.

29. The method of claim 25, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; and depositing a second conductivity type semiconductor material on the gate dielectric.

30. A method of forming a semiconductor memory device, comprising:
forming at least one memory array;
forming a number of wordlines coupled to the memory array;
forming a number of bitlines coupled to the memory array;
forming at least one transistor coupled to the memory array comprising:
forming a first gate dielectric layer on a semiconductor substrate;
forming a first conductivity type semiconductor layer on top of the first gate dielectric layer;
selectively removing a portion of the first conductivity type semiconductor layer to expose the first gate dielectric, the portion defining a first conductivity type well region;
forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well;

depositing a second conductivity type semiconductor material on the second gate dielectric layer and forming a first conductivity type gate from the first conductivity type semiconductor layer; and

forming source/drain regions adjacent the gate.

31. The method of claim 30, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the first gate dielectric layer, before removing the first gate dielectric layer.

32. The method of claim 30, further comprising coupling a hardened dielectric layer to the second gate dielectric layer.

33. The method of claim 30, wherein the second gate dielectric layer differs in thickness from the first gate dielectric layer.

34. The method of claim 30, wherein the first conductivity type semiconductor layer is formed in-situ.

35. The method of claim 30, wherein the second conductivity type semiconductor layer is formed in-situ.

36. The method of claim 30, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; removing the first gate dielectric layer; and depositing a second conductivity type semiconductor material on the second gate dielectric layer.

37. A method of forming a semiconductor memory device, comprising:

forming at least one memory array;

forming a number of wordlines coupled to the memory array;

forming a number of bitlines coupled to the memory array;

forming a pair of transistors coupled to the memory array comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

depositing a second conductivity type semiconductor layer on the gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.

38. The method of claim 37, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the gate dielectric layer.

39. The method of claim 37, wherein the first conductivity type semiconductor layer is formed in-situ.

40. The method of claim 37, wherein the second conductivity type semiconductor layer is formed in-situ.

41. The method of claim 37, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; and depositing a second conductivity type semiconductor layer.

42. A method of forming a semiconductor memory device, comprising:

forming at least one memory array;

forming a number of wordlines coupled to the memory array;

forming a number of bitlines coupled to the memory array;

forming a pair of transistors coupled to the memory array comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a first gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the first gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to expose the first gate dielectric, the

portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well;

depositing a second conductivity type semiconductor layer on the second gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.

43. The method of claim 42, wherein forming a first conductivity type semiconductor well comprises implanting a first conductivity type well through the first gate dielectric layer, before removing the first gate dielectric layer.

44. The method of claim 42, further comprising coupling a hardened dielectric layer to the second gate dielectric layer.

45. The method of claim 42, wherein the second gate dielectric layer differs in thickness from the first gate dielectric layer.

46. The method of claim 42, wherein the first conductivity type semiconductor layer is formed in-situ.

47. The method of claim 42, wherein the second conductivity type semiconductor layer is formed in-situ.

48. The method of claim 42, wherein a single mask is used for selectively removing a portion of the first conductivity type semiconductor layer; forming a first conductivity type semiconductor well; removing the first gate dielectric layer; and depositing a second conductivity type semiconductor material on the second gate dielectric layer.

49. A method of forming an integrated circuit, comprising:

forming a buried channel transistor on a semiconductor substrate comprising:

forming a base region in the semiconductor substrate using a base region lithography mask;

forming an emitter region in the base region using an emitter lithography mask;

forming a surface channel transistor on the semiconductor substrate comprising:

forming a first conductivity type gate region in the semiconductor substrate; and

forming a second conductivity type gate region using the emitter region lithography mask.

50. The method of claim 49, wherein the first conductivity type gate region and the second conductivity type gate region are formed from doped poly silicon that was deposited in-situ.